REMARKS

Reconsideration of the above-identified patent application in view of the amendments above and the remarks following is respectfully requested.

Claims 1-3, 5-8, 10-23 and 26-32 are in this case. Claims 1-3, 5-8, 10-23 and 26-32 have been rejected under § 103(a). Independent claims 1 and 31 have been canceled. Dependent claims 2, 3, 5 and 6 have been amended. New independent claim 33 and new dependent claims 34-43 have been added.

The claims before the Examiner are directed toward methods of assembling and testing electronic devices, specifically, systems-in-package (SIPs), and to a device so assembled and tested. A CPU, a nonvolatile memory and a volatile memory are fabricated on respective, physically independent chips and are packaged together in a common package with the CPU operationally connected to the memories. Testing programs, for testing the memories by writing to the memories, are stored in the nonvolatile memory and are executed by the CPU from the volatile memory to test the memories. Then the CPU is tested. The results of the tests of the memories are stored in the nonvolatile memory.

§ 103(a) Rejections – Chesley '142 in view of AAPA

The Examiner has rejected claims 1-5, 7, 8, 10-16, 18-21, 23, 26 and 27 under § 103(a) as being "unpatented" (Applicant presumes the Examiner meant "unpatentable") over Chesley, US Patent No. 4,333,142 (henceforth, "Chesley '142") in view of Applicant Admitted Prior Art (henceforth, "AAPA"). The Examiner's rejection is respectfully traversed.

Chesley '142 teaches a computer fabricated on a single wafer **11** with redundant components and configured to test itself when power is applied to identify

and not use inoperative components. Specifically, the computer includes many CPU chips **12**, many ROM chips **13** and many RAM chips **14**. When power is applied to the computer, each CPU tests itself until a working CPU is found. The working CPU does checksum testing of the ROMs until a working ROM is found. The working CPU then runs a test routine stored in the working ROM to test itself and also runs another test routine stored in the working ROM to test the RAMs in order to identify working RAMs.

The AAPA cited by the Examiner is fabricating a CPU and one or more memories on separate chips and assembling and packaging the chips in a SIP.

Claims 1 and 31 have been canceled, thereby rendering moot the Examiner's rejection of these claims.

Applicant respectfully submits that the Examiner has failed to establish *prima facie* obviousness of the remaining independent claims.

According to MPEP 2143.03, in order for *prima facie* obviousness of a claim to be established, all the claim limitations must be taught or suggested by the cited references. This is not the case with regard to independent claims 7, 18, 23, 26, 29, 30 and 32.

In the cases of independent claims 7, 30 and 32, the prior art cited by the Examiner fails to teach or suggest steps (e) and (f) of claim 7, steps (d) and (e) of claim 30 and steps (e) and (f) of claim 32: loading a testing program into the volatile memory and testing one of the memories (claims 7 and 32) or testing the volatile memory (claim 30) by using the CPU to execute the loaded program. A CPU chip **12** of Chesley '142 tests a ROM chip **13** by summing the words of the ROM chip **13** and comparing the sum to a checksum stored in the ROM chip **13**. The check sum routine that the CPU chip **12** executes is "permanently built into the logic of each CPU"

(column 3 lines 15-16). A CPU chip **12** of Chesley '142 tests a RAM chip **14** by executing a RAM test program that is stored in a ROM chip **13**. As best understood, both the check sum routine and the RAM test program are executed in place and are not loaded into a RAM chip **14** for execution. The cited AAPA is confined to fabricating a CPU and one or more memories on separate chips and assembling and packaging the chips in a SIP and is silent about how the memories are tested.

Similar arguments were presented in response to the Office Action mailed July 14, 2006. In reply, the Examiner has directed Applicant's attention to column 3 lines 17-28 of Chesley '142 and has commented:

> Here the RAM is the volatile memory and when the CPU uses line 26 to "WRITE" on to the RAM it is in an essence loading the test program.

Applicant respectfully disagrees. As best understood, the purpose of line **26** is to write data to a RAM chip **14** during normal operation of the computer of Chesley '142 after the good RAM chips **14** have been found, as described in column 3 lines 55-58:

> The RAM's are utilized as a page allocated memory system in which data and program space is allocated on demand on a page basis, with each RAM module corresponding to one page.

There is neither a hint nor a suggestion in Chesley '142 of loading any code from a ROM chip **13** to a RAM chip **14** for execution. In particular, the check sum routine cannot be loaded into a RAM chip **14** for execution because the check sum routine is executed only to test ROM chips **13** before any RAM chips **14** are accessed. As stated in column 3 lines 47-49,

> Once a good ROM and a good CPU are found, the CPU uses a RAM test routine contained in the ROM to test each RAM module in sequence. (emphasis added)

In the case of independent claim 18 the prior art cited by the Examiner fails to teach or suggest the limitation recited in step (d) that the testing program tests the nonvolatile memory by steps including writing to the nonvolatile memory. The nonvolatile memories of Chesley 142 are ROM chips **13** that inherently are read-only and cannot be written to. The cited AAPA is confined to fabricating a CPU and one or more memories on separate chips and assembling and packaging the chips in a SIP and is silent about how the memories are tested.

In the case of independent claim 23 the prior art cited by the Examiner fails to teach or suggest the limitation recited in element (a) that the nonvolatile memory has stored therein a testing program for testing itself. In Chesley '142 the check sum routine that the CPU chip **12** executes to test ROM chips **13** is "permanently built into the logic of each CPU" (column 3 lines 15-16). ROM chips **13** store only CPU test programs and RAM test programs. The cited AAPA is confined to fabricating a CPU and one or more memories on separate chips and assembling and packaging the chips in a SIP and is silent about how the memories are tested.

Similar arguments were presented in response to the Office Action mailed July 14, 2006. In reply, the Examiner has directed Applicant's attention to column 3 lines 7-14 of Chesley '142 and has commented:

> Here, the ROM is the non-volatile memory, and the CPU is performing a "test function" to test the ROM. The ROM "contains" test program and check sum, which are used to test the ROM.

Applicant respectfully disagrees. The ROM contains the check sum but not the test program. As noted above, the check sum routine is "permanently built into the logic of each CPU" (column 3 lines 15-16).

In the case of independent claims 26 and 29 the prior art cited by the Examiner fails to teach or suggest step (f) of claim 26 and step (g) of claim 29: storing, in the

nonvolatile memory, results of testing the volatile memory. The nonvolatile memories of Chesley '142 are ROM chips **13** that inherently are read-only and cannot be written to. The results of testing the volatile memories of Chesley '142 (RAM chips **14**) are stored in address register **28** of the first good CPU chip **12**. The cited AAPA is confined to fabricating a CPU and one or more memories on separate chips and assembling and packaging the chips in a SIP and is silent about how the memories are tested.

Similar arguments were presented in response to the Office Action mailed July 14, 2006. In reply, the Examiner has directed Applicant's attention to column 1 lines 45-47 of Chesley '142 and has commented:

> Here again the non volatile memory is the ROM and the volatile memory is the RAM, whose test results can be stored in the CPU registers, or in "another suitable store". Within the context of Chesley "suitable store" can be interpreted to be the ROM because these are the only three memory components in the prior art and it would be advantageous to store the results in the ROM to prevent data loss upon a power failure.

Applicant respectfully disagrees. As noted above, the nonvolatile memories of Chesley '142 are ROM chips **13** that inherently are read-only and cannot be written to. The "other suitable store" need not be nonvolatile; in fact the example of an "other suitable store" presented by Chesley '142 himself, in column 3 lines 50-52, is one of RAM chips **14**:

> ...a table of the addresses of the good and bad RAM's is created in the first good RAM.

With independent claims 7, 18 and 26 allowable in their present form it follows that claims 8, 10-16, 19-21 and 27 that depend therefrom also are allowable.

With independent claim 1 now canceled, claims 2-6 have been amended to depend from claim 29 rather than from claim 1. Because claim 29 recites storing the results of the testing specifically in the nonvolatile memory, claim 5 has been

amended to recite reading the stored results from the nonvolatile memory. With independent claim 29 allowable in its present form it follows that claims 2, 3 and 5 that depend therefrom also are allowable.

§ 103(a) Rejections – Chesley '142 in view of AAPA and further in view of Takizawa '663

The Examiner has rejected claims 6, 17, 22 and 28 under § 103(a) as being unpatentable over Chesley '142 in view of AAPA and further in view of Takizawa, US Patent No. 6,198,663. The Examiner's rejection is respectfully traversed.

It is demonstrated above that independent claims 7, 18, 26 and 29 are allowable in their present form. It follows that claims 6, 17, 22 and 28 that depend therefrom also are allowable.

New Claims

New independent claim 33 is claim 29 without the step of testing the CPU, as this step is not needed to distinguish the present invention from the cited prior art. New dependent claims 34 and 35 correspond to the claims (3 and 6) that depend from claim 29 and do not recite a limitation of the testing of the CPU.

New dependent claims 36-43 limit their respective independent claims to a single CPU, in contrast to Chesley '142 who needs multiple CPU chips **12** because he does not know in advance which CPU chip **12** will work. Support for this limitation is found in the specification in the Figure that shows a single CPU **12** in SIP **10**.

Drawings

Attached please find a formal replacement drawing, as required by the Examiner.

In view of the above amendments and remarks it is respectfully submitted that independent claims 7, 18, 23, 26, 29, 30, 32 and 33, and hence dependent claims 2, 3, 6, 8, 10-17, 19-22, 27, 28 and 34-43 are in condition for allowance. Prompt notice of allowance is respectfully and earnestly solicited.

Respectfully submitted,

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